Amendments to the Claims:

Please amend the claim as follows in a complete set of the claims.

Claims (complete set).

1. (Currently amended) A chip comprising:

a receiver to receive a full cycle encoded signal in which data is represented in data time segments and no data time segment has more than one cycle, and provides a data output signal responsive to the full cycle encoding signal, wherein the receiver is to further receive a complementary full cycle encoded signal and wherein the receiver provides the data output signal responsive to the full cycle encoded signal and the complementary full cycle encoded signal, further comprising a synchronizing circuit to synchronize the data output signal to a second periodic signal and wherein the synchronizing circuit includes a periodic signal deriving circuit to provide a first periodic signal in response to the full cycle encoded signal and wherein the first periodic signal is used in the synchronizing.

2. (Original) The chip of claim 1, wherein within some of the data time segments the full cycle encoded signal is the inverse of the cycle encoded signal within others of the data time segments, and wherein within some of the data time segments the full cycle encoded signal constitutes one cycle and within others of the data time segments the full cycle encoded signal constitutes a half cycle.

3. (Canceled)

4. (Currently amended) The chip of claim [[3]] 1, wherein the receiver includes an initial receiving circuit to compare the full cycle encoded signal and the complementary full cycle encoded signal to provide a received signal in response thereto, and the receiver includes a delay circuit to provide at least two delayed signals which are delayed versions of the received signal, and a logic circuit to provide the data output signal responsive to the delayed signals.

5. (Original) The chip of claim 4, wherein the logic circuit also provides an inverse data output signal.

6. (Original) The chip of claim 4, wherein the logic circuit responds to changes the received signal at the beginning of a data time segment, but not to mid-data time segment changes in the received signal.

7. (Previously presented) The chip of claim 4, wherein the at least two delay signals

include a ¼ data time segment delay signal and a ¾ data time segment delay signal.

8. (Original) The chip of claim 4, wherein the logic circuit includes an exclusive-OR gate to receive the at least two delayed signals and the logic circuit includes first and second flip-flips to receive an output of the exclusive-OR gate and to receive the received signal at clock inputs of the first and second flip-flops, wherein the first flip-flop is clock on a rising edge and the second flip-flop is clocked on a falling edge.

9. (Currently amended) The chip of claim 4, wherein the logic circuit includes an AND gate that receives outputs of ~~the~~ first and second flip-flops and the data output signal is an output of the AND gate.

10. (Original) The chip of claim 4, wherein the logic circuit includes a state machine that provides an output control signal to control at least one multiplexer circuit to control whether the data output signal is from a first flip-flop or a second flip-flop.

11. (Canceled)

12. (Previously presented) The chip of claim 1, wherein the receiver includes an initial receiving circuit to compare the full cycle encoded signal and a reference signal to provide a received signal in response thereto, and the receiver includes a delay circuit to provide at least two delayed signals which are delayed versions of the received signal, and a logic circuit to provide the data output signal responsive to the delayed signals.

13. (Previously presented) The chip of claim 12, wherein the at least two delay signals include a ¼ data time segment delay signal and a ¾ data time segment delay signal.

14. (Currently amended) A chip comprising:

a receiver to receive a cycle encoded signal in which data is represented in data time segments and at least some data time segments do not have more than one cycle, and to ~~provides~~ provide a data output signal responsive to the cycle encoded signal; and

a synchronizing circuit to synchronize the data output signal to a second periodic signal and wherein the synchronizing circuit includes a periodic signal deriving circuit to provide a first periodic signal in response to the cycle encoded signal and wherein the first periodic signal is used in the synchronizing.

15. (Currently amended) The chip of claim 14, wherein the cycle encoded signal is a full cycle encoded signal in which no data time segment has more than one cycle of an encoding signal.

16. (Currently amended) The chip of claim [[14]] 15, wherein within some of the data time segments the full cycle encoded signal is the inverse of the cycle encoded signal within others of the data time segments, and wherein within some of the data time segments the full cycle encoded signal constitutes one cycle and within others of the data time segments the full cycle encoded signal constitutes a half cycle.

17. (Currently amended) The chip of claim 14, wherein the receiver ~~that~~ includes an initial receiving circuit to receive the cycle encoded signal and provide a received signal in response thereto, a delay circuit to provide delayed signals which are delayed versions of the received signal and a logic circuit to provide [[a]] the data out signal responsive to the delayed signals which includes recovered data from the cycle encoded signal.

18. (Currently amended) The chip of claim 17, wherein the logic circuit also provides an inverse of the data output signal.

19. (Original) The chip of claim 17, wherein the logic circuit responds to changes the received signal at the beginning of a data time segment, but not to mid-data time segment changes in the received signal.

20. (Previously presented) The chip of claim 17, wherein the logic circuit includes an AND gate that receives outputs of first and second flip-flops and the data output signal is an output of the AND gate.

21. (Previously presented) The chip of claim 17, wherein the logic circuit includes a state machine that provides an output control signal to control at least one multiplexer circuit to control whether the data output signal is from a first flip-flop or a second flip-flop.

22. (Currently amended) The chip of claim 14, wherein the receiver ~~is to~~ further receive a complementary cycle encoded signal and wherein the receiver provides the data output signal responsive to the cycle encoded signal and the complementary cycle encoded signal.

23. (Previously presented) The chip of claim 22, wherein the receiver includes an initial receiving circuit to compare the cycle encoded signal and the complementary cycle encoded signal to provide a received signal in response thereto, and the receiver includes a delay circuit to provide at least two delayed signals which are delayed versions of the received signal, and a logic circuit to provide the data output signal responsive to the delayed signals.

24. (Original) The chip of claim 23, wherein the logic circuit responds to changes the received signal at the beginning of a data time segment, but not to mid-data time segment

changes in the received signal.

25. (Original) The chip of claim 23, wherein the logic circuit includes an exclusive-OR gate to receive the at least two delayed signals and the logic circuit includes first and second flip-flips to receive an output of the exclusive-OR gate and to receive the received signal at clock inputs of the first and second flip-flops, wherein the first flip-flop is clock on a rising edge and the second flip-flop is clocked on a falling edge.

26. (Canceled)

27. (Currently amended) The chip of claim 14, wherein within some of the data time segments the cycle encoded signal is at the same voltage at a beginning and an end of the data time ~~segment~~ segments, and wherein within some of the data time segments the cycle encoded is at the same voltage at a beginning, middle, and end of the data time segments, and wherein within some of the data time segments the cycle encoded signal is an inverse of the cycle encoded signal within others of the data time segments.

28. (Currently amended) A system comprising:

a transmitter including:

(a) a cycle encoding circuit to receive a data input signal and to provide a cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals; and

(b) a complementary cycle encoding circuit to receive the data input signal and to provide a complementary cycle encoded signal in response thereto by continuously joining portions of the different encoding signals; and

a receiver to receive the cycle encoded signal and the complementary cycle encoded signal and to recover values of the data input signal in response thereto to provide a data output signal, wherein the receiver includes an initial receiving circuit to compare the cycle encoded signal and the complementary ~~full~~ cycle encoded signal to provide a received signal in response thereto, and the receiver includes a delay circuit to provide at least two delayed signals which are delayed versions of the received signal, and a logic circuit to provide the data output signal which represents the recovered values, wherein the logic circuit provides the data output signal responsive to the delayed signals, wherein the logic circuit includes an exclusive-OR gate to receive the at least two delayed signals and the logic circuit includes first and second flip-flips to

receive an output of the exclusive-OR gate and to receive the received signal at clock inputs of the first and second flip-flops, wherein the first flip-flop is clock on a rising edge and the second flip-flop is clocked on a falling edge.

29. (Original) The system of claim 28, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

30. (Previously presented) The system of claim 28, wherein the cycle encoded signal is a full cycle encoded signal and the complementary cycle encoded signal is a complementary full cycle encoded signal in which no data time segment has more than one cycle of an encoding signal.

31. (Original) The system of claim 28, wherein the logic circuit responds to changes the received signal at the beginning of a data time segment, but not to mid-data time segment changes in the received signal.

32. (Canceled)

33. (Original) The system of claim 28, further comprising a synchronizing circuit to synchronize the data output signal to a second periodic signal and wherein the synchronizing circuit includes a periodic signal deriving circuit to provide a first periodic signal in response to the cycle encoded signal and wherein the first periodic signal is used in the synchronizing.